

<b>Notice of References Cited</b>	Application/Control No. 10/063,626	Applicant(s)/Patent Under Reexamination HUANG, ANDY	
	Examiner Ayal I. Sharon	Art Unit 2123	Page 1 of 2

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,928,626	08-2005	McGaughy et al.	716/1
	B	US-6,931,609	08-2005	Naruta et al.	716/4
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hamoui, A.A. et al. "An Analytical Model for Current, Delay, and Power Analysis of Submicron CMOS Logic Circuits." IEEE Transactions on Circuits and Systems II: Analog and Digital DSP. Oct. 2000. Vol. 47, Issue 10, pp. 999-1007.
	V	"Level 27 SOSFET Model." Star-Hspice Manual – Release 1999.4 Dec. 15, 1999. Printed from <a href="http://siloam.han.ac.kr/~young/data/hspice_html/hspice-152.html">http://siloam.han.ac.kr/~young/data/hspice_html/hspice-152.html</a> .
	W	Alinikula, P. et al. "Design of Class E Power Amplifier with Non-linear Parasitic Output Capacitance." IEEE Transactions on Circuits and Systems II: Analog and Digital DSP. Feb. 1999. Vol. 46, Issue 2, pp. 114-119.
	X	Ma, S.W. et al. "Piece-Wise Linear Approximation of MOS Nonlinear Junction Capacitance in High-Frequency Junction Capacitance in High-Frequency Class E Amplifier Design." 2003 IEEE Conf. on Electron Device and Solid-State Circuits. Dec. 16-18, 2003. pp

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	Examiner Ayal I. Sharon	Art Unit 2123	Page 2 of 2

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	A	US-			
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	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Enz, C. "An MOS Transistor Model for RF IC Design Valid in All Regions of Operation." IEEE Transactions on Microwave Theory and Techniques. Jan. 2002. Vol.50, Issue 1. pp.342-359.
	V	Bisdounis, L. "Analytical Transient Response and Propagation Delay Evaluation of the CMOS Inverter for Short-Channel Devices." IEEE Journal of Solid State Circuits. Feb. 1998, Vol.33, Issue 2, pp.302-306.
	W	Ismail, M. et al. "Finite GB and MOS Parasitic Capacitance Effects in a Class of MOSFET-C Filters." Proc. of the 33rd Midwest Symposium on Circuits and Systems. Aug.12-14, 1990. Vol.2, pp.938-941.
	X	Boothroyd, A.R. et al. "MISNAN – A Physically Based Continuous MOSFET Model for CAD Applications." IEEE Transactions on CAD of Integrated Circuits and Systems. Dec. 1991. Vol.10, Issue 12. pp.1512-1529.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.